CIGRE WG B4.57 and B4.58

DC GRID TEST SYSTEM

PART II:

AVERAGE-VALUE MODELS (TYPE 5)

DCS1 test system in DIgSILENT PowerFactory

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Abstract

This document describes the DIgSILENT PowerFactory model of the CIGRE DC Grid Test System number 1 (DCS1) [1] and its parameters for dynamic and transient stability studies. This paper is a continuation of earlier and preliminary work that can be found in [2], where the model and results of the steady state implementation were covered. All dynamic models and their parameters will be described and detailed throughout the paper. Results of the dynamic studies are given, and time-varying signals are presented in plots as a guide for final users.

1. General description

The CIGRE DC Grid Test System working group has developed three different benchmark cases for steady state and transient studies: "DCS1", "DCS2" and "Full Test System".

In this paper, the model corresponding to topology "DCS1" has been upgraded with the implementation of the control and protection system dynamic models Type 5 in DIgSILENT PowerFactory.

Average-value models (Type 5) are used to model the converters, avoiding the use of a detailed representation of VSC-HVDC systems with the IGBTs in EMT-type programs, forcing the use of a very small integration time-step size to compute switching events in an accurate manner. Average-value models are more efficient and provide similar dynamic averaged response. The MMC behaviour is represented using controlled voltage and current sources. Low level control systems are not considered, and simulations are then faster than the detailed equivalent model (Type 4).

Average-value models are used to perform transient studies involving large disturbances on AC grids. The design and tuning of high level control systems can also be achieved with Type 5 simulation models [1].

The **"DCS1"** system topology represents a DC system and provides a suitable model to perform investigations about a single point-to-point link. It consists of a HVDC link of +/-200 kV which connects two AC grids,

one it's an offshore wind power plant and the other one it's an onshore grid. These AC grids are modelled as a Thevenin equivalent which parameters are defined in Appendix A (Table 1). Furthermore, it includes two AC/DC converters based on MMC topology. Detailed data can be found in [2].

The inclusion of frequency dependent effects in DC lines for time domain simulations has been solved using a rational approximation by vector fitting [3]. In general, DC cables are represented by single pi-equivalent circuits or multiple pi-equivalents, that neglect the frequency-dependent effects and could lead to a wrong stability assessment. In the proposed implementation of the DCS1 benchmark, the cable is modelled with multiple parallel RL-branches, as proposed in [4], improving the dynamics of the cable and its impact at DC system level.

2. Control and protection systems

The structure for the control and protection systems is presented in Figure 1. The control system of both MMC converters and the protection logic to trip the breaker are defined through a frame object, where each slot represents different lower level functions:

- **Measurement slots:** both the AC and DC voltages at the MMC terminals are measured. Also, active and reactive powers which are exported from the MMC to the AC busbar are measured.
- **Outer control loop:** it transforms the different setpoints into current reference signals in the dq axis.
- **Inner control loop:** The inner control loop limits reference current signals into an acceptable range and corrects the controlled signals with the inner current controller. The modulation factors obtained will define the performance of the MMC.

2.1. Outer control loops

The outer control loop is subdivided in two parts: one responsible for the D-axis control and the other for the Q-axis.

The D-axis outer controller implements different control modes:

- **DC voltage control mode:** it compares the measured DC voltage with a reference value, obtaining an error which is corrected by a PI controller (Figure 2).
- **Active power control mode:** it compares the measured active power against a desired reference value, calculating an error which is corrected by the PI controller. Furthermore, it includes a droop control as well as a protection system which attempts to maintain the voltage inside a suitable range (Figure 3).

The Q-axis outer controller implements different control modes:

- **Reactive power control mode:** it compares the measured reactive power at AC terminals with a desired reference value, obtaining an error which is corrected by a PI controller (Figure 4).
- **AC voltage control mode:** it compares the measured AC voltage with a reference value, obtaining an error which is corrected by a PI controller (Figure 5).

The following subsections provide a more detailed description of the inner control loop, the outer control loop and additional model functions.

2.2. Current limiter

The scope of the current limiter is to limit both the D-axis and the Q-axis reference current values. A strategy to prioritize active or reactive current setpoints is implemented. When the vector summation of input current setpoints exceeds the

maximum limiting apparent current, the current of one of the axes is limited according to the priority defined by the end user.

2.3. Inner control loops

The inner controller (Figure 6) controls the converter AC voltage that will be used to generate the modulated switching pattern. It compares the measured current values in both axes with their respective reference values, obtaining an error which is corrected by a PI controller for every axis component. Additionally, the ri to dq transformation block converts imaginary and real measured AC voltage signals into dq voltage signals.

2.4. Protection system

The protection system is responsible for the supervision of current and voltage variations. The current protection function compares the measured DC current from the MMC to a maximum pre-defined value. When the measured DC current exceeds the reference limit value, the protection triggers a signal to block the converter instantaneously. Following the blocking of the converter, the circuit breaker will be opened after a pre-defined delay. Both the circuit breaker triggering time and the MMC blocking time are adjustable.

The voltage protection function compares the measured voltage with the undervoltage threshold. If the measured voltage drops below the reference limit value, the converter will be blocked after a pre-defined time.

All parameters needed to set up the control and protection system models and their block diagrams can be found in Appendix A and B respectively.

3. Simulation results

The tests proposed in [1] have been reproduced in DIgSILENT PowerFactory 2018SP1 (x64). Test results are presented in this document as a guide for the final user, as in the reference document. Three different test cases are described, and results are presented in Appendix C:

Test Case 1, AC fault at Ba-A1: A 3-phase to ground metallic fault is applied during 200ms at bus Ba-A1 (Figure 9).
Test case 2, AC fault at Bo-C1: A 3-phase to ground metallic fault is simulated during 200ms at bus Bo-C1 (Figure 15).
Test case 3, DC fault at Bm-A1: A permanent pole-to-pole metallic fault is simulated at Cm-A1 terminals (Figure 20).

4. References

[1] C. W. G. B4.57, Guide for the development od Models for HVDC Converters in a HVDC Grid, December 2014.

[2] U. C. 3. M. DIgSILENT Ibérica, PART I: LOAD FLOW MODEL in DIgSILENT PowerFactory, 2016.

[3] B. Gustavsen and A. Semlyen, "Rational approximation of frequency domain responses by vector fitting," *IEEE Transactions of Power Delivery,* vol. 14, no. 3, pp. 1052-1061, July 1999.

[4] J. Beerten, S. D'Arco and J. A. Suul, "Frequency-dependent cable modelling for small-signal stability analysis of VSC-HVDC systems," *IET Generation, Transmission & Distribution,* vol. 10, no. 6, pp. 1370-1381, 2016.

Appendix A: Model parameters

Table 1: Generation configuration in test system "DCS1"

Generation	Bus	Nominal Voltage in KV	Short Circuit Power in GVA	R/X Ratio	Type	Control	Set points
Ext_Grid_A1	Ba-A1	380	30	0.1	Voltage source	V	1.00 p.u.
						φ	0.00 °
Ext_Grid_C1	Bo-C1	145	8	0.1	Voltage source	V	1.00 p.u.
						φ	0.00 °

Table 2: Control mode AC/DC converters in test system "DCS1"

AC/DC Converter	Control	Set points	Voltage and angle control	Power flow control	
			Controlled Buses	Bus From	Bus To
Cm-A1	V_{DC}	1.00 p.u.	Bm-A1_pos/Bm-A1_neg	-	-
	Q	0 Mvar	-	AC_Cm-A1 Grid	AC_Cm-A1 Conv
Cm-C1	P	400 MW	-	AC_Cm-C1 Grid	AC_Cm-C1 Conv
	Q	0 Mvar	-	AC_Cm-C1 Grid	AC_Cm-C1 Conv

Table 3: Parameter values - current controller model

Parameter	Value	Unit
I_kp	0.48	p.u./p.u.
I_ki	149.00	s^{-1}
ωL	0.255	p.u.
Pmmax	1.5	p.u.
ed_min	-1.5	p.u.
eq_min	-1.5	p.u.
ed_max	1.5	p.u.
eq_max	1.5	p.u.

Table 4: Parameter values - active power controller model

Parameter	Value	Unit
Vdc_min_db	0.95	p.u.
Vdc_max_db	1.05	p.u.
Vdc_kp_db	10.00	p.u./p.u.
P_min	-1.2	p.u.
P_max	1.2	p.u.
P_ki	33.00	s^{-1}
P_kp	0	p.u./p.u.
kdroop	0	p.u./p.u.
Tfilt	0.01	s

Table 5: Parameter values - protection system model

Parameter	Value	Unit
idc_limit	3	p.u.
ac_BRK_delay	0.04	s
Block_MMC_delay1	$40*10^{-6}$	s
Vac_limit	0.1	p.u.
Block_MMC_delay2	0.02	s

Table 6: Parameter values - reactive power controller model

Parameter	Value	Unit
Q_min	-0.5	p.u.
Q_max	0.5	p.u.
Q_ki	33.00	s^{-1}
Q_kp	0	p.u./p.u.
Tfilt	0.01	s

Table 7: Parameter values - Vac controller model

Parameter	Value	Unit
Vac_ki	30	s^{-1}
Vac_kp	0	p.u./p.u.
Tfilt	0.01	S
Vac_min	-0.5	p.u.
Vac_max	0.5	p.u.

Table 8: Parameter values - Vdc controller model

Parameter	Value	Unit
Vdc_ki	272.00	s^{-1}
Vdc_kp	8.00	p.u./p.u.
Tfilt	0.01	s
Vdc_min	-1.2	p.u.
Vdc_max	1.2	p.u.

Table 9: Parameter values – Idq ref limiter

Parameter	Value	Unit
I_lim	1.1	p.u.

Table 10: Parameter values – dq transformation

Parameter	Value	Unit
Tfilt	0.01	s

Appendix B: Dynamic Models

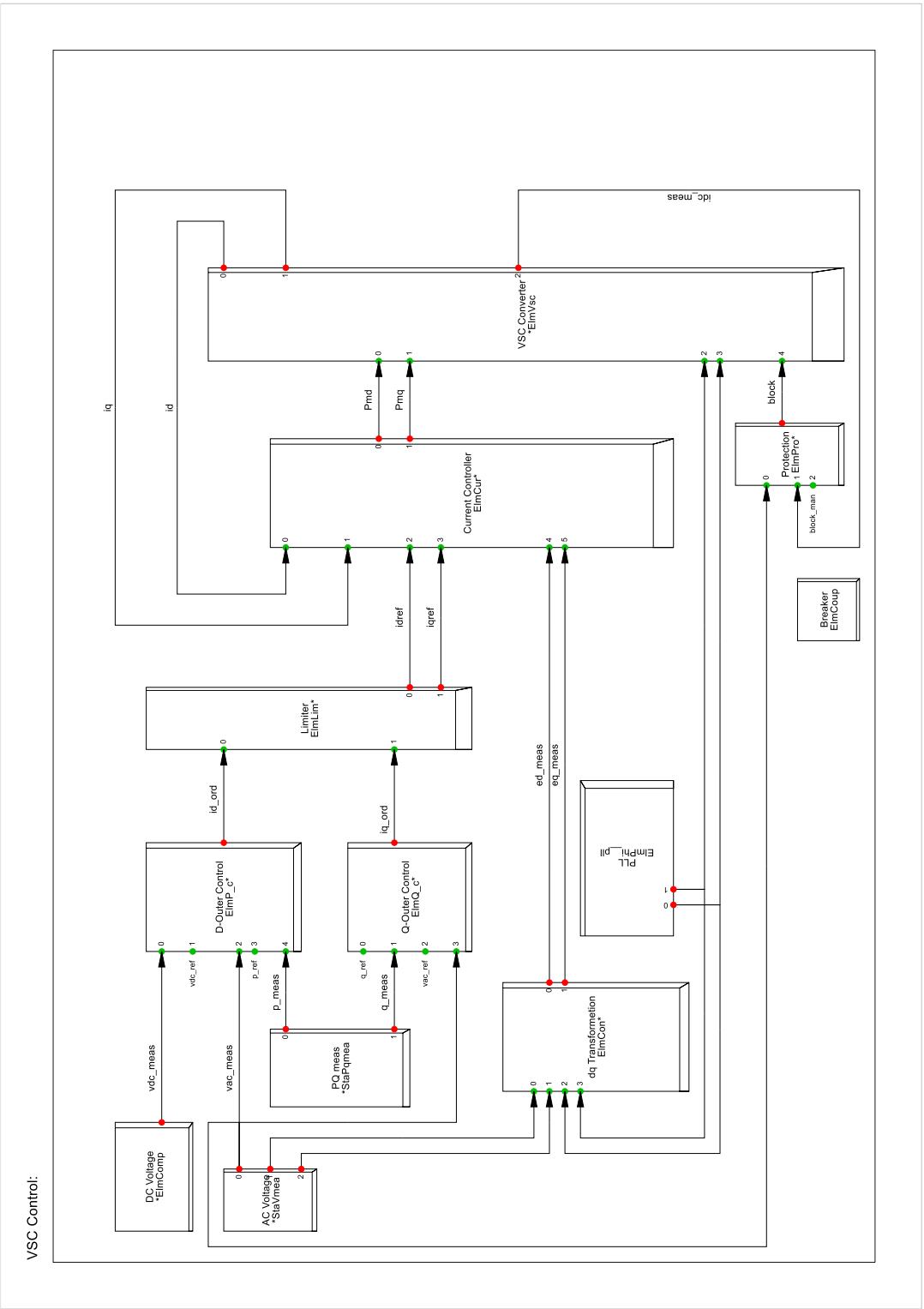

Figure 1: General view of control and protections systems

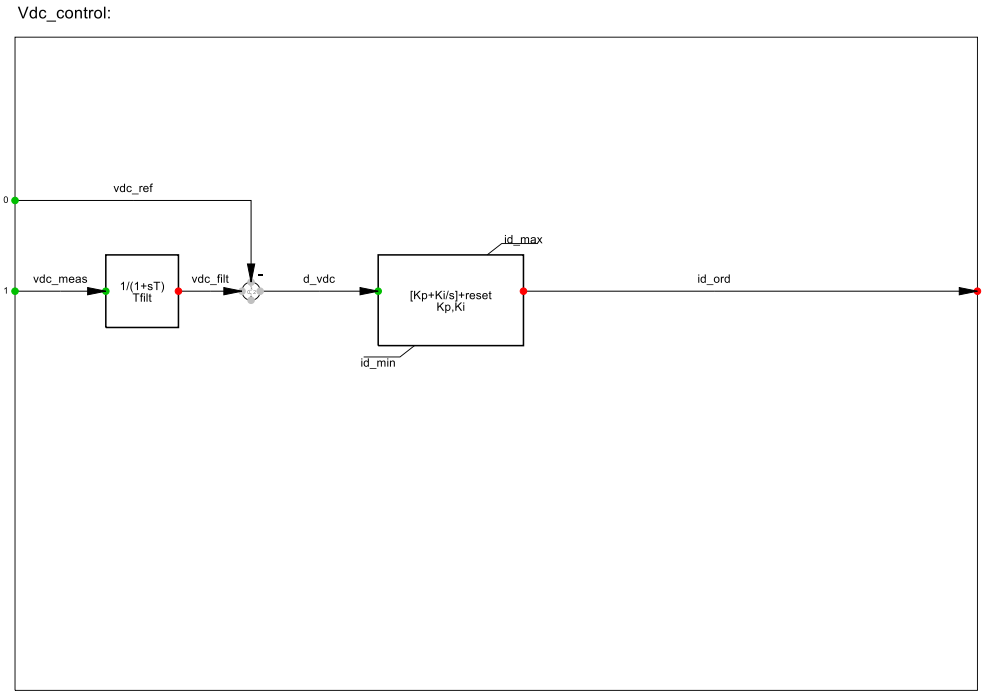

Figure 2: DC voltage controller model

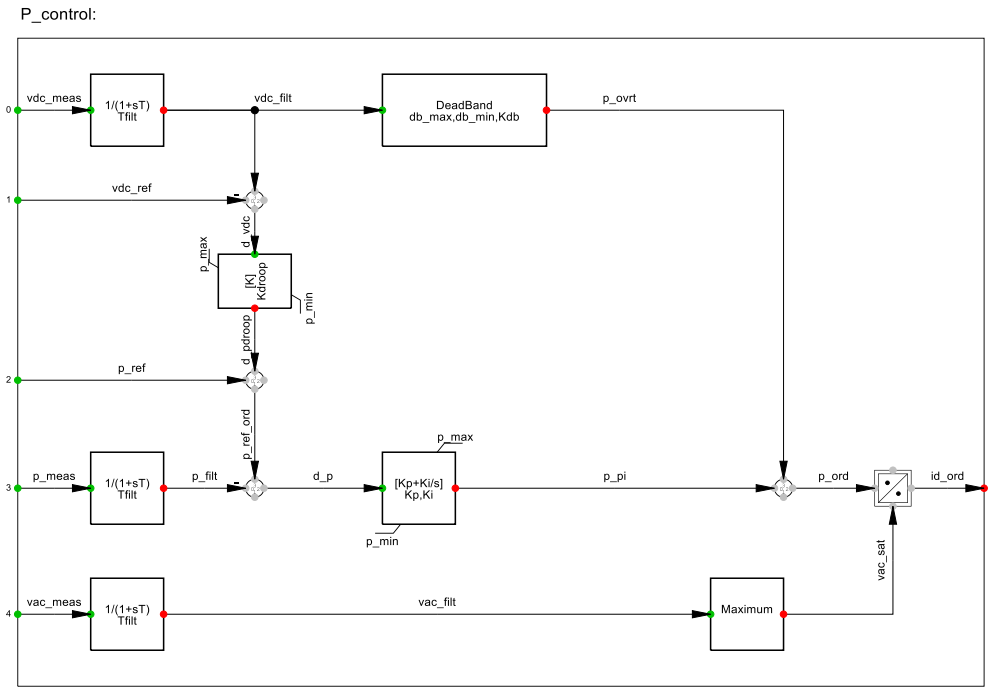

Figure 3: Active power controller model

Q_control:

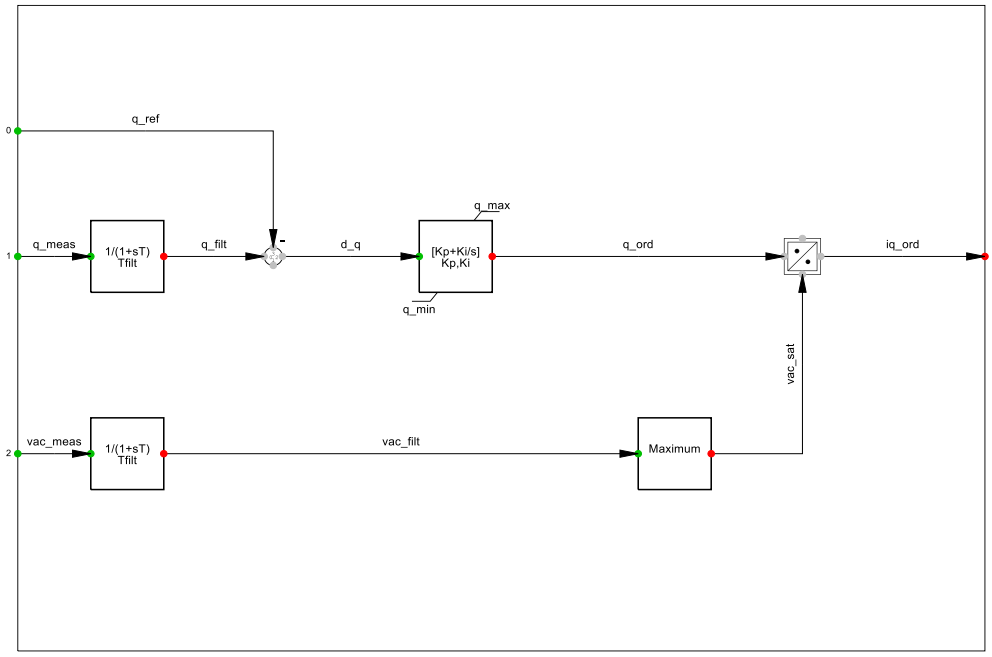

Figure 4: Reactive power controller model

Vac_control:

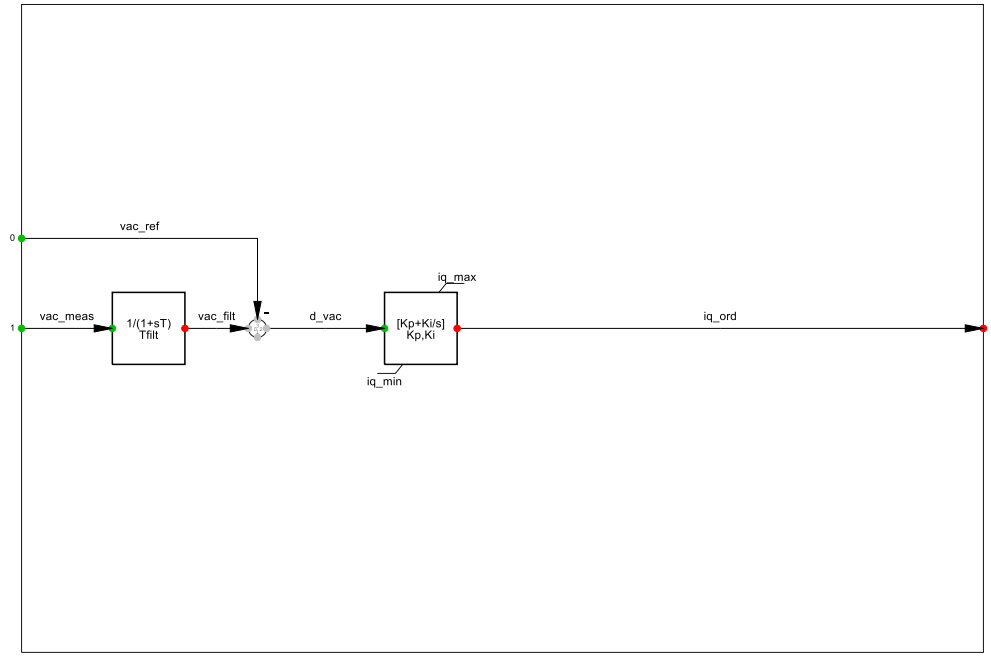

Figure 5: AC voltage controller model

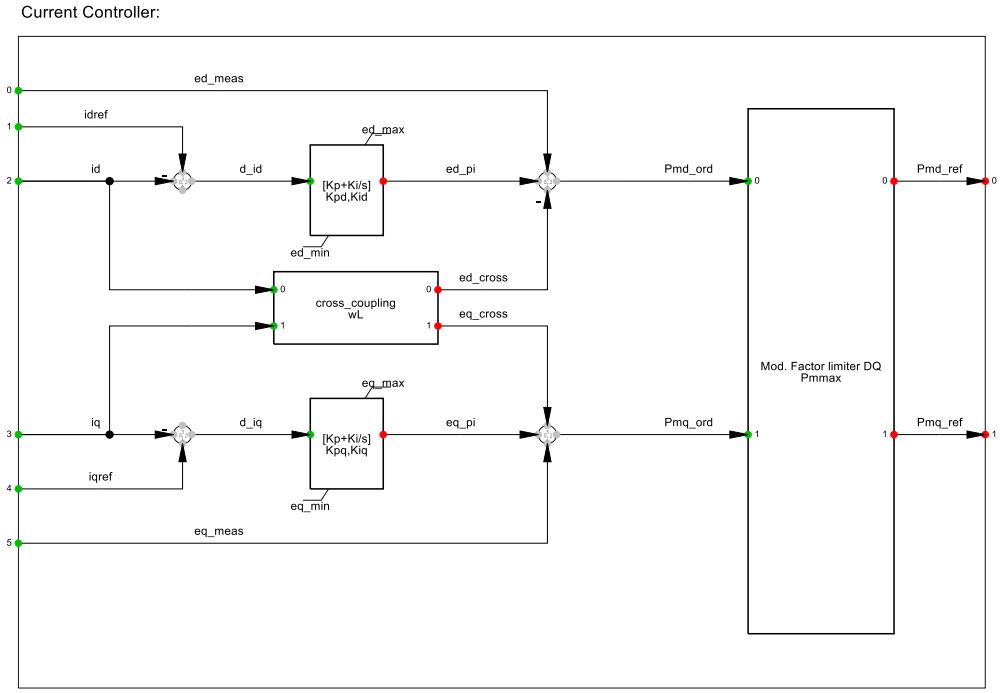

Figure 6: Current controller model

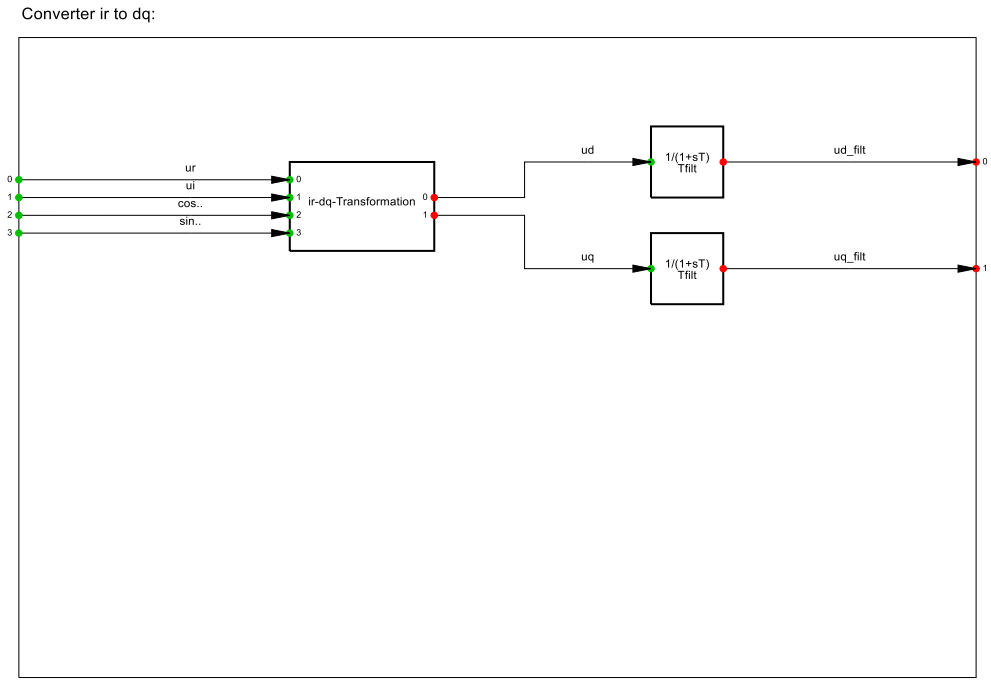

Figure 7: RI to DQ transformation

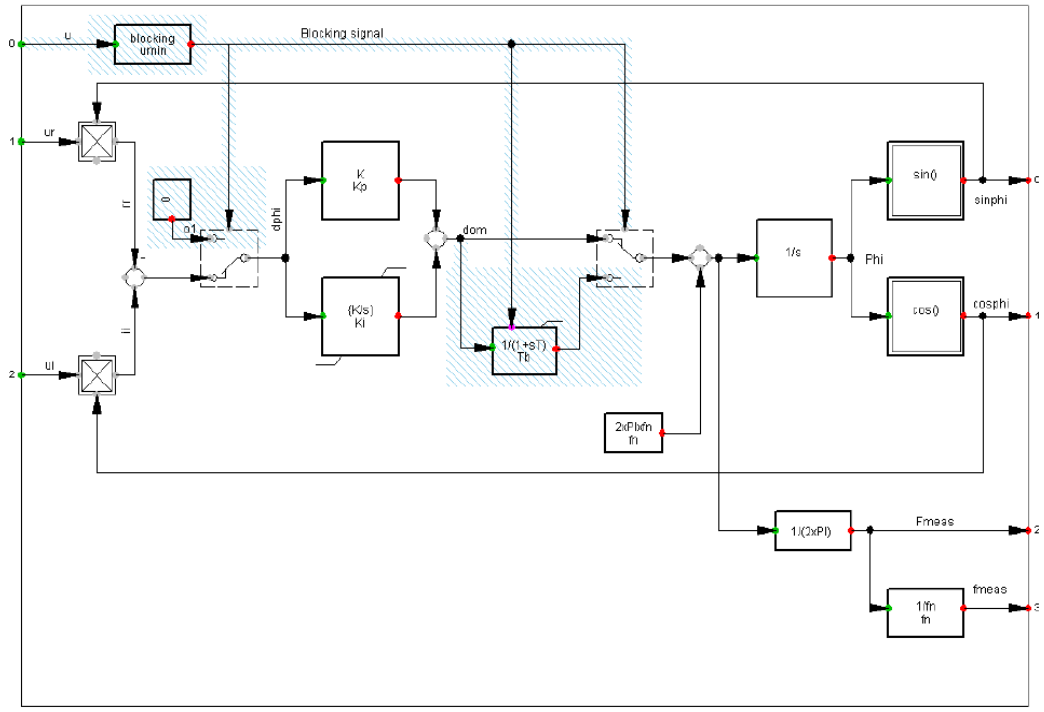

Figure 8: DIgSILENT PLL block diagram

Appendix C: Dynamic Model Results

Test Case 1: AC fault at Ba-A1

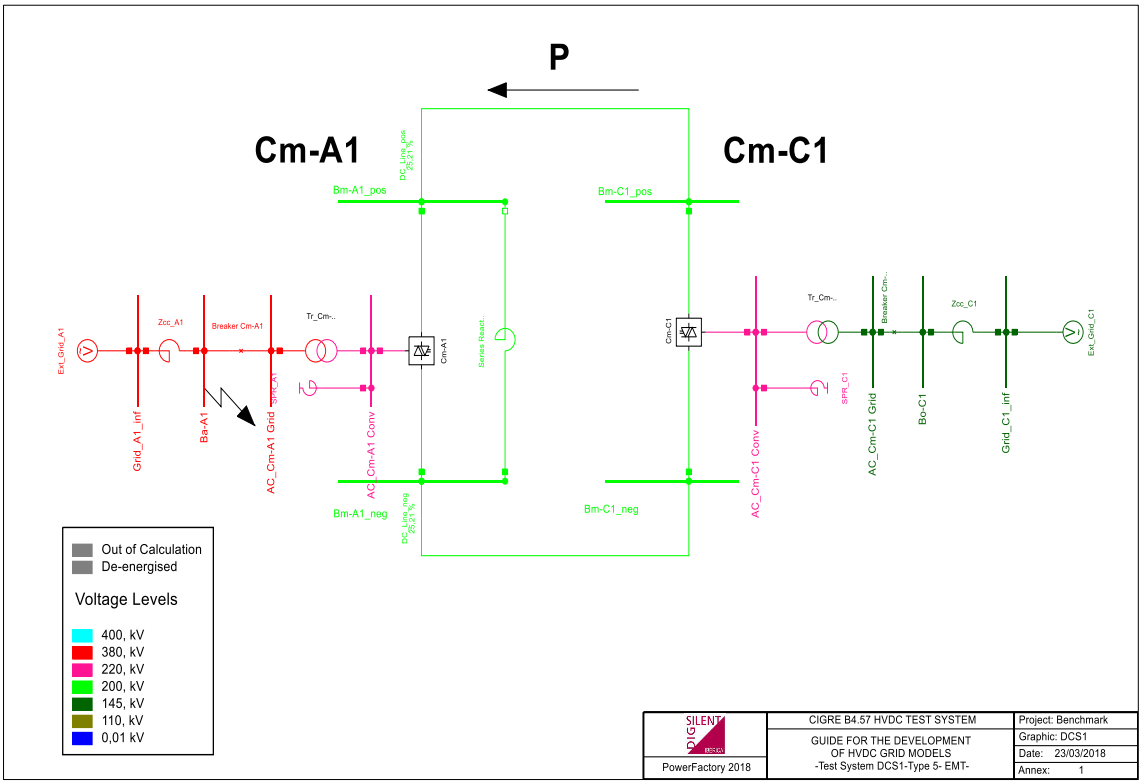

Figure 9: AC fault at busbar Ba-A1 in DCS1

Table 11: AC fault at busbar Ba-A1 – Events

Events	Time (ms) After fault application
AC fault (applied at 1s)	0
Cm-A1 blocking due to low AC voltage	20
Cm-C1 deadband activation	23
AC fault elimination	200
Cm-A1 deblocking	244
Cm-C1 deadband de-activation	266

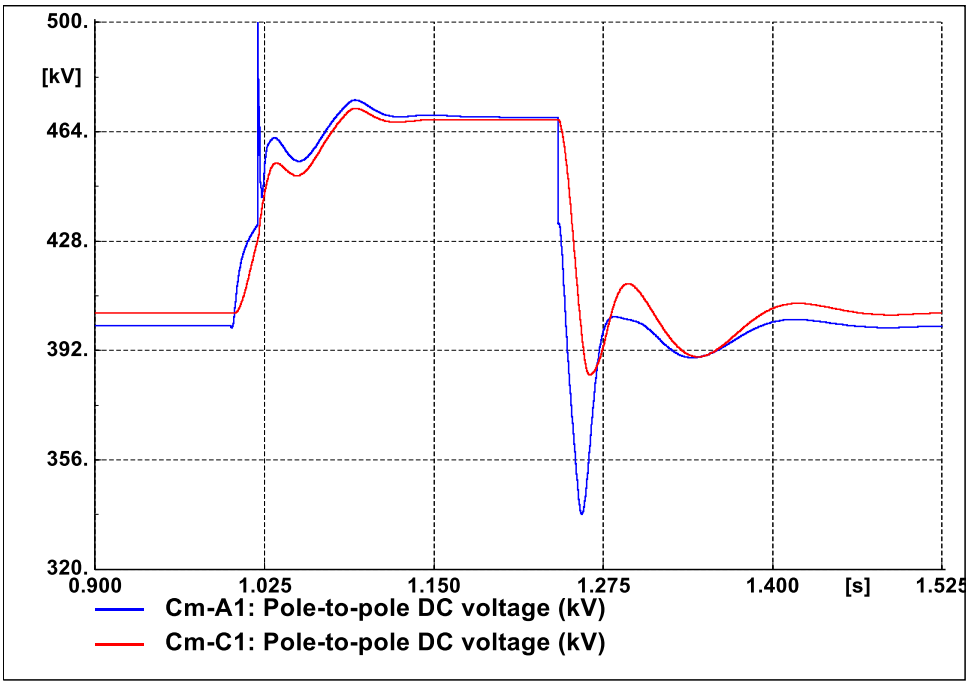

Figure 10: Pole-to-pole DC voltage at converter terminals Cm-A1 and Cm-C1

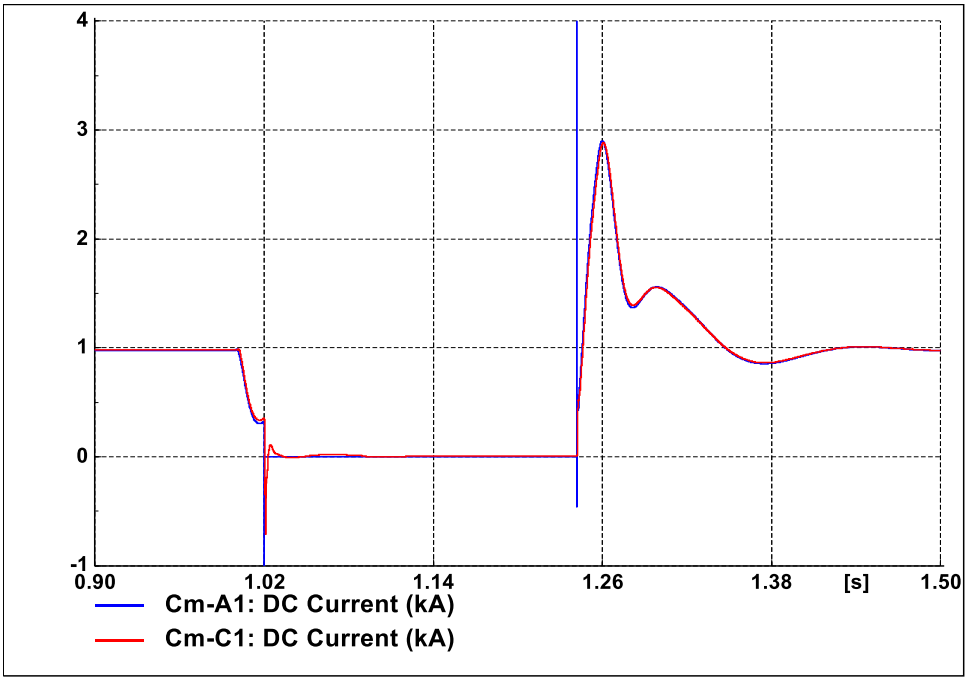

Figure 11: DC current at converter terminals Cm-A1 and Cm-C1

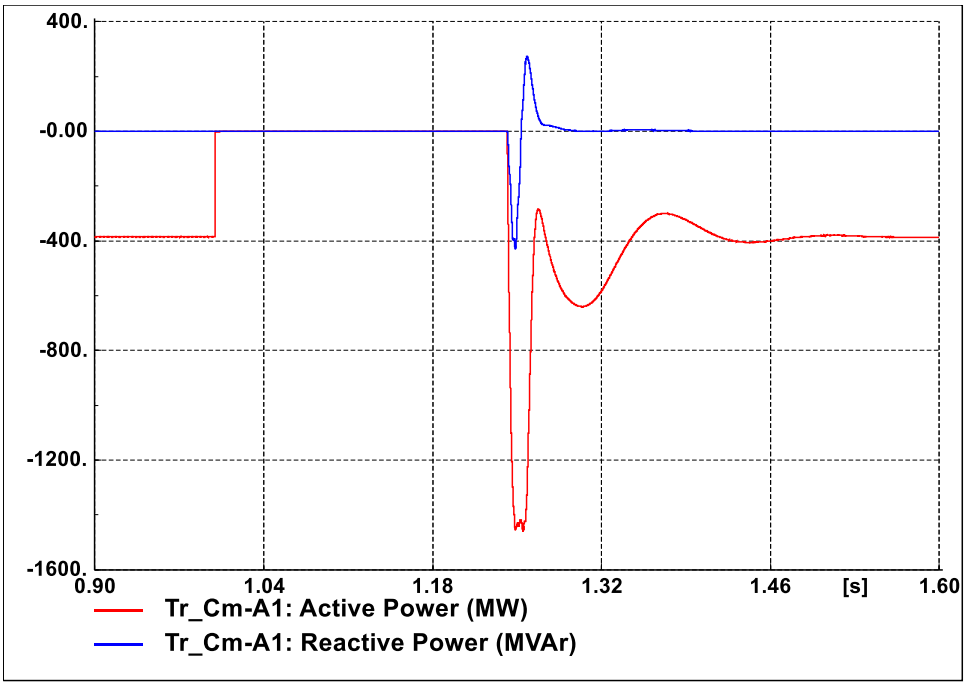

Figure 12: Active & Reactive power flow on primary side of transformer Cm-A1

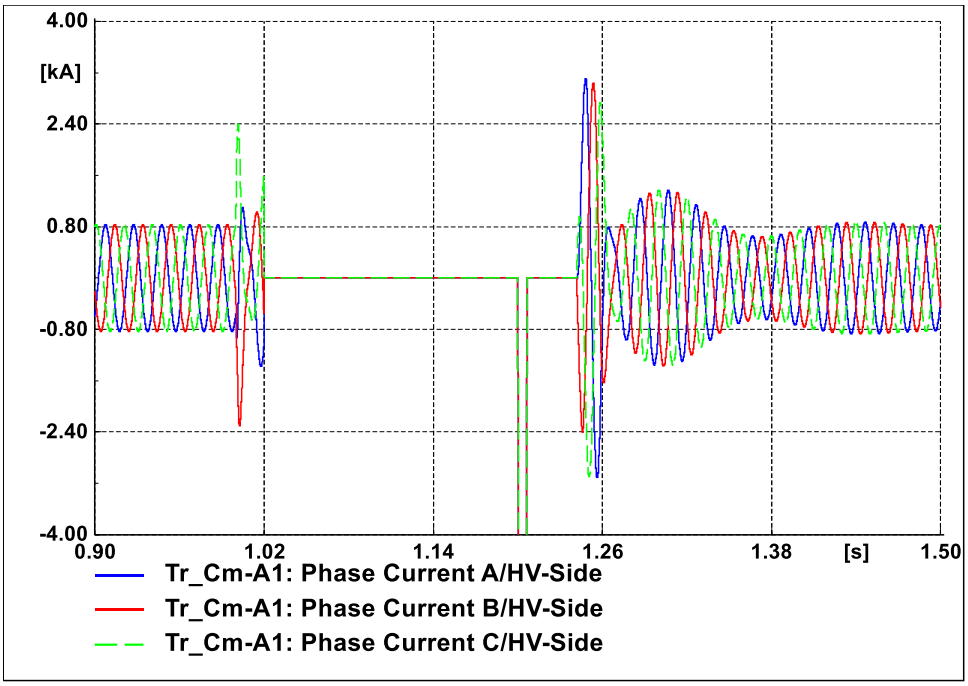

Figure 13: 3-phase instantaneous currents on primary side of transformer Cm-A1

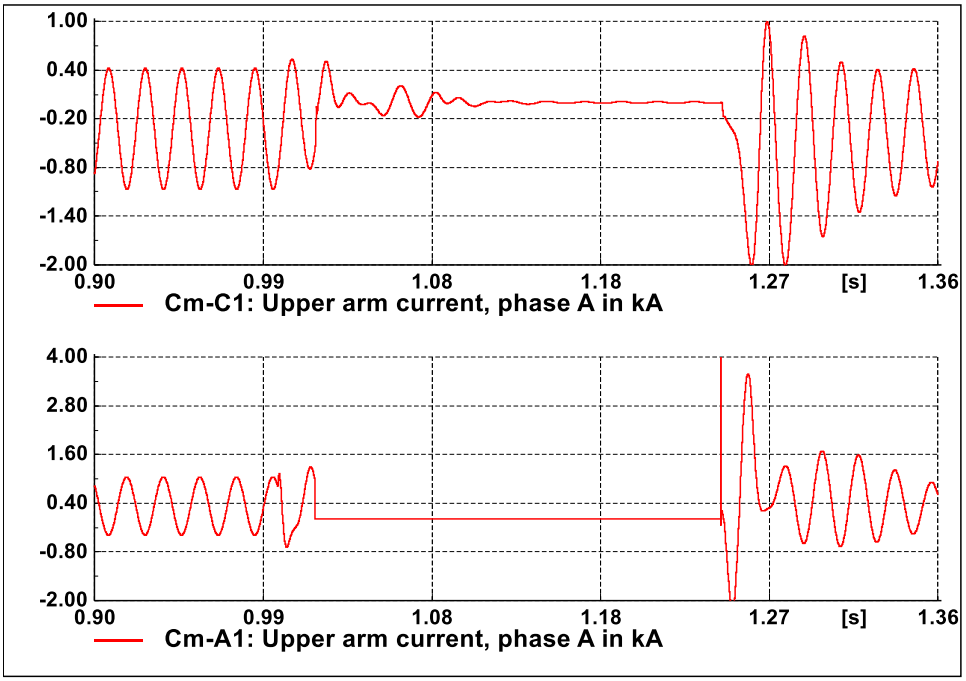

Figure 14: Instantaneous current flowing in upper valve phase A (top: Cm-C1, bottom: Cm-A1)

Test Case 2: AC Fault at Bo-C1

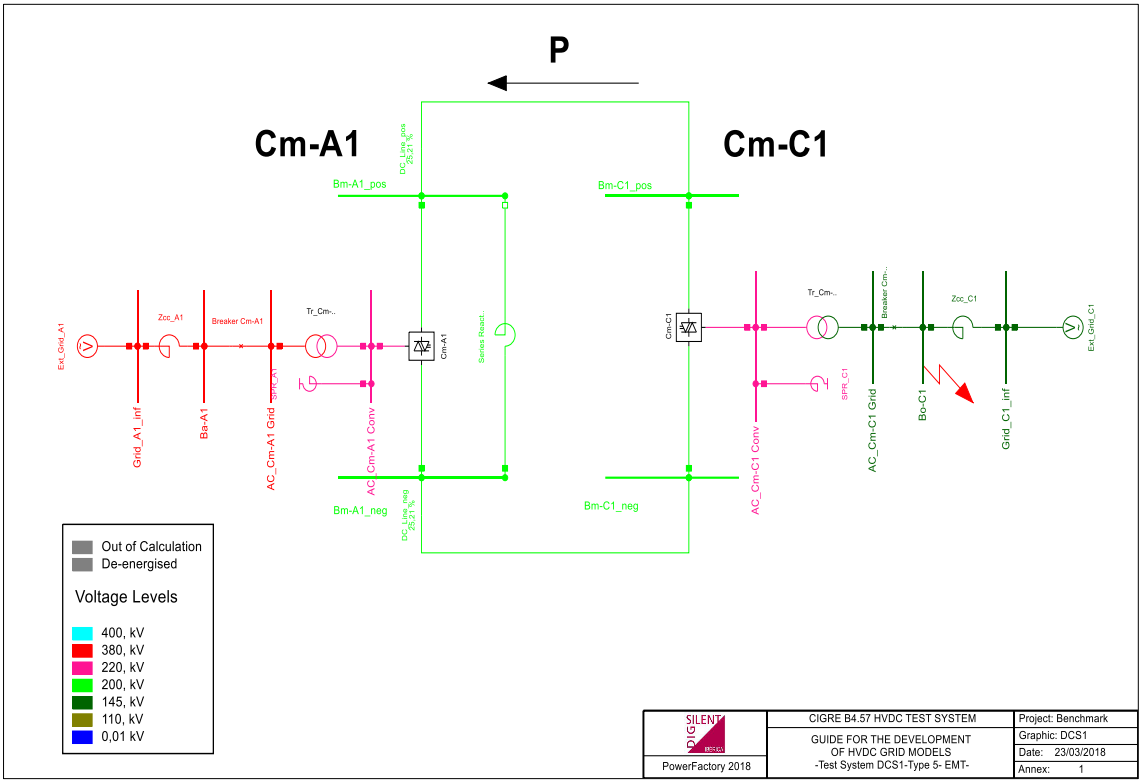

Figure 15: AC Fault at Bo-C1 in DCS1

Table 12: AC Fault in Bo-C1 - Events

Events	Time (ms) After fault application
AC fault (applied at 1s)	0
Cm-C1 blocking due to low AC voltage	20
AC fault elimination	200
Cm-C1 deblocking	244

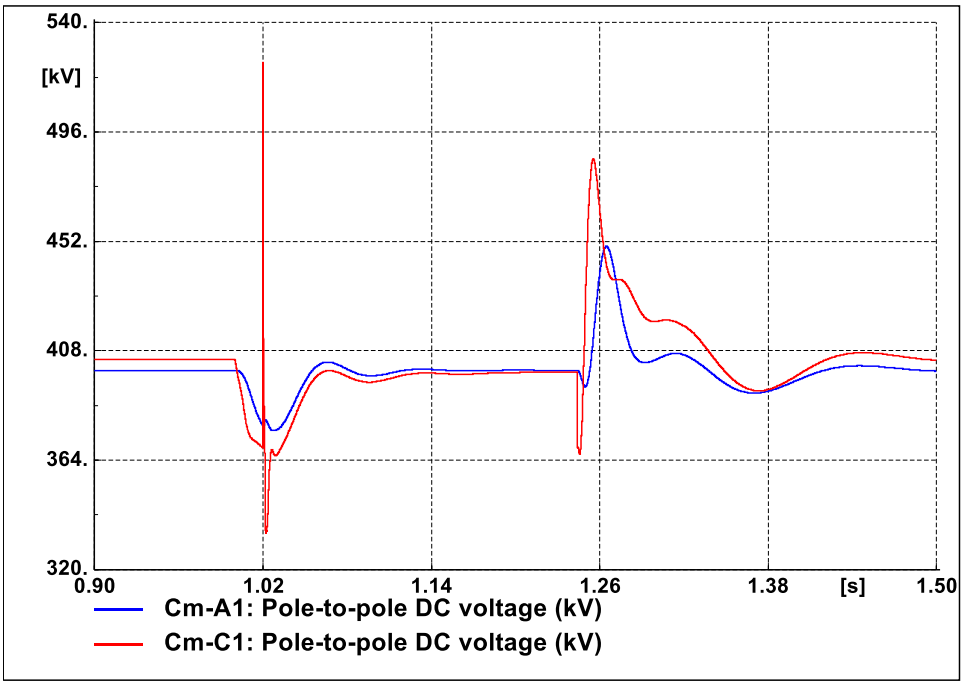

Figure 16: Pole-to-pole DC voltage at converter terminals Cm-A1 and Cm-C1

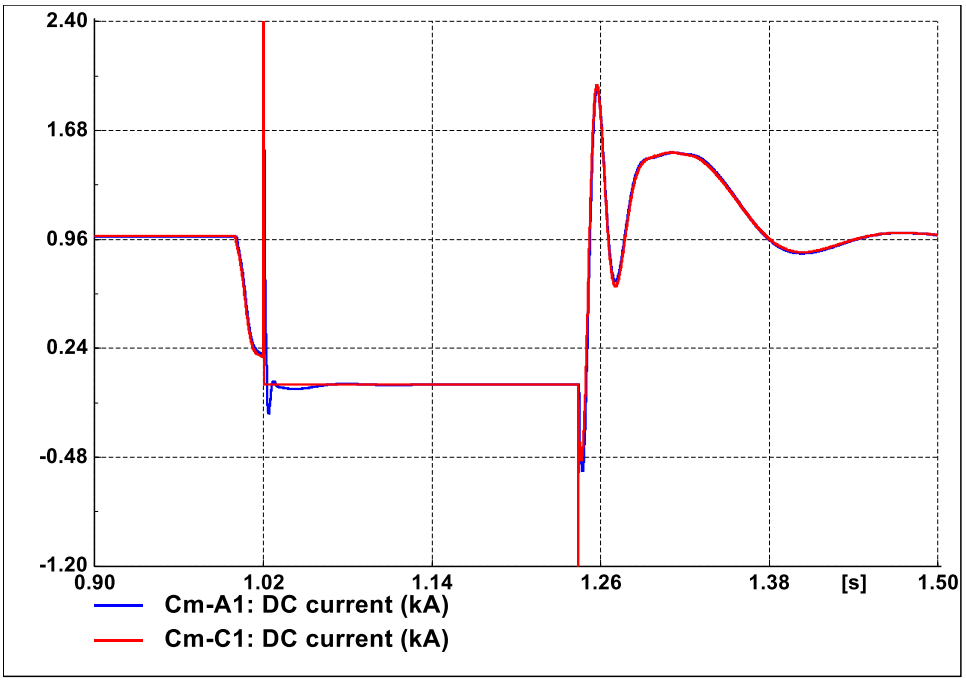

Figure 17: DC current at converter terminals Cm-A1 and Cm-C1

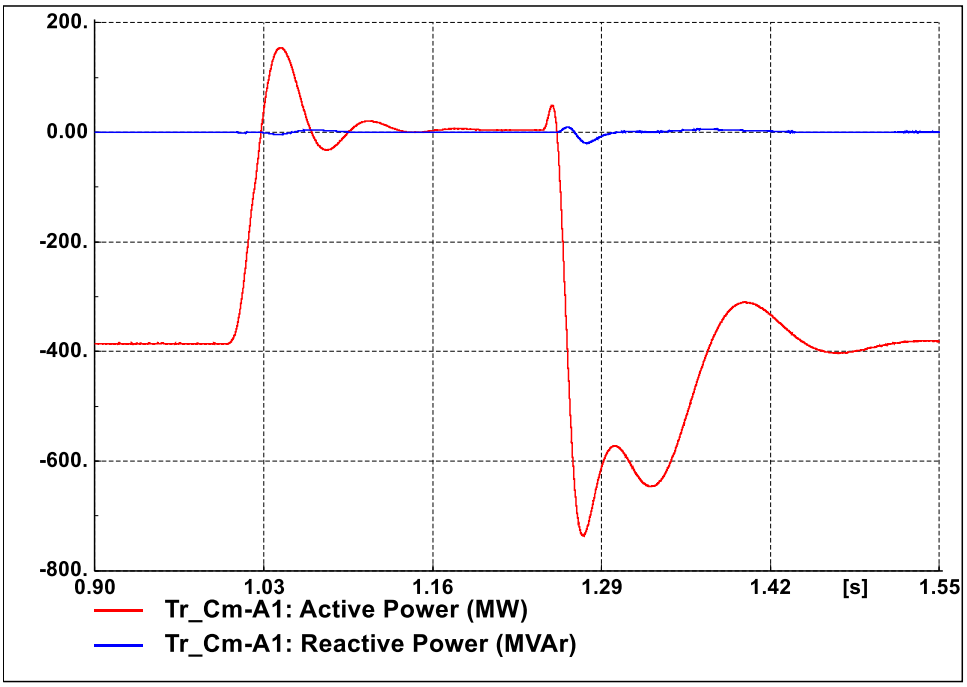

Figure 18: Active & reactive power flow on primary side of transformer Cm-A1

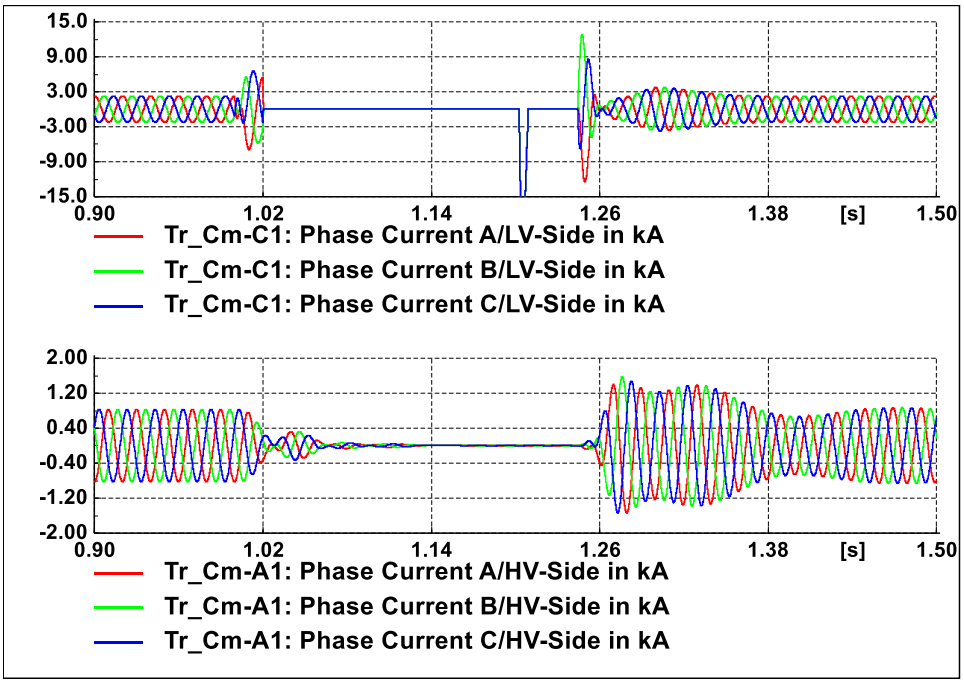

Figure 19: 3-phase instantaneous currents on primary side of transformer Cm-C1 (top) and Cm-A1 (bottom)

Test Case 3: DC Fault at Bm-A1

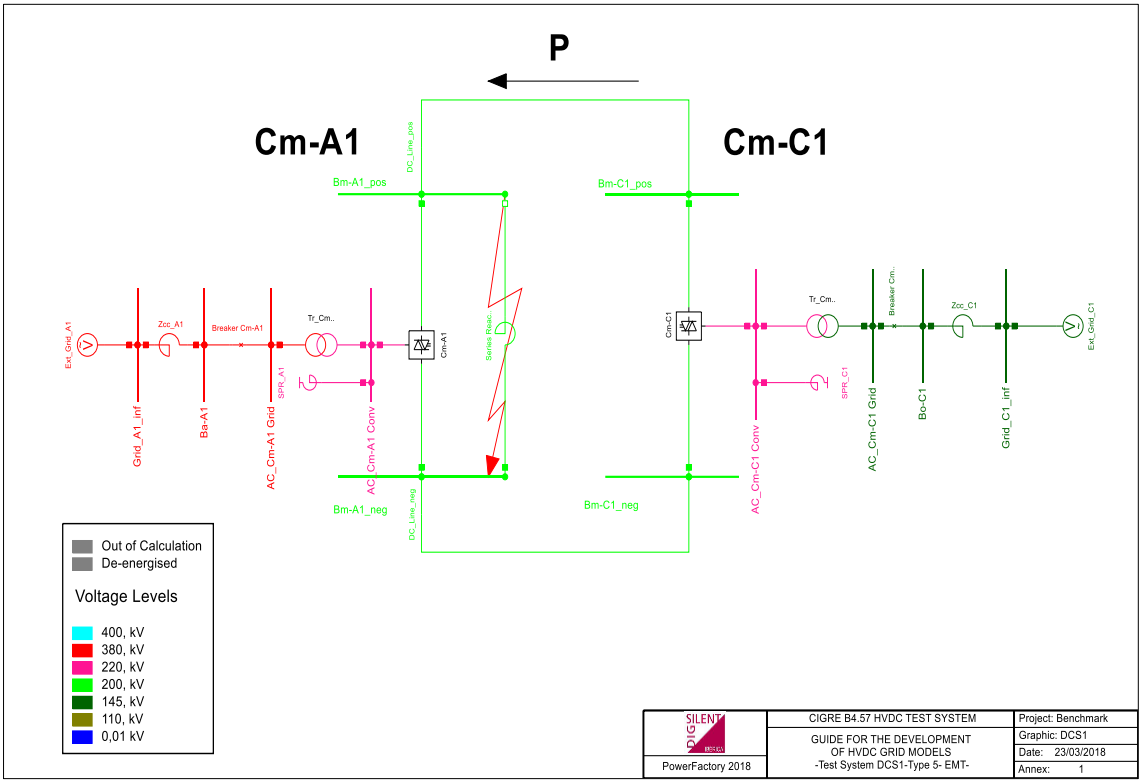

Figure 20: DC Fault at Bm-A1 in DCS1

Table 13: DC Fault at Bm-A1 - Events

Events	Time (ms) After fault application
DC fault (applied at 1s)	0
Cm-A1 blocking due to DC overcurrent	0.061
Cm-C1 blocking due to DC overcurrent	1.133
AC Circuit Breaker opens (Cm-A1)	40
AC Circuit Breaker opens (Cm-C1)	47

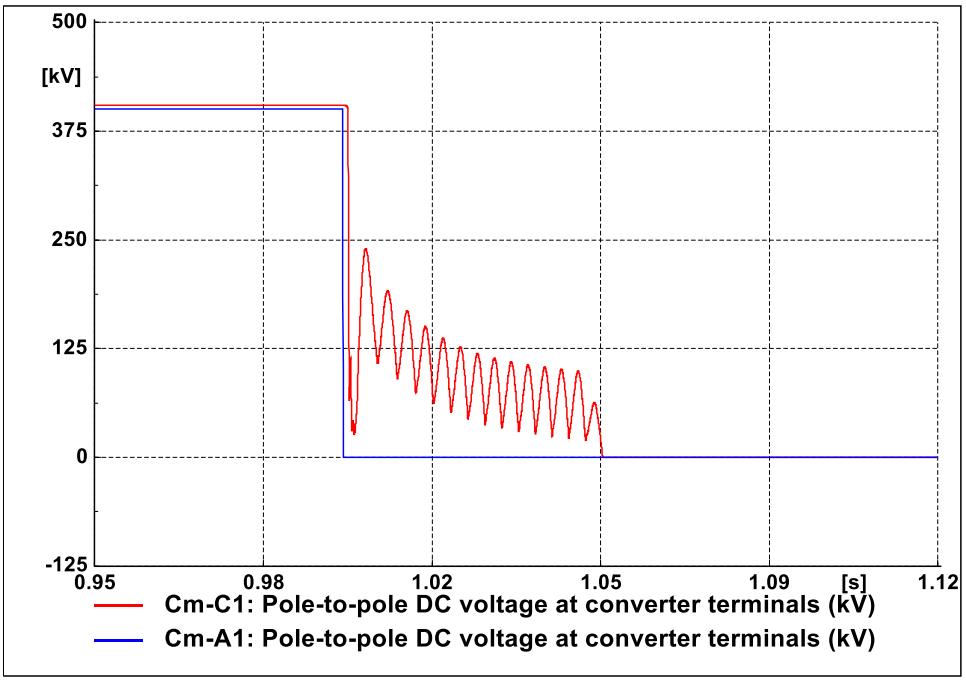

Figure 21: Pole-to-pole DC voltage at converter terminals Cm-A1 and Cm-C1

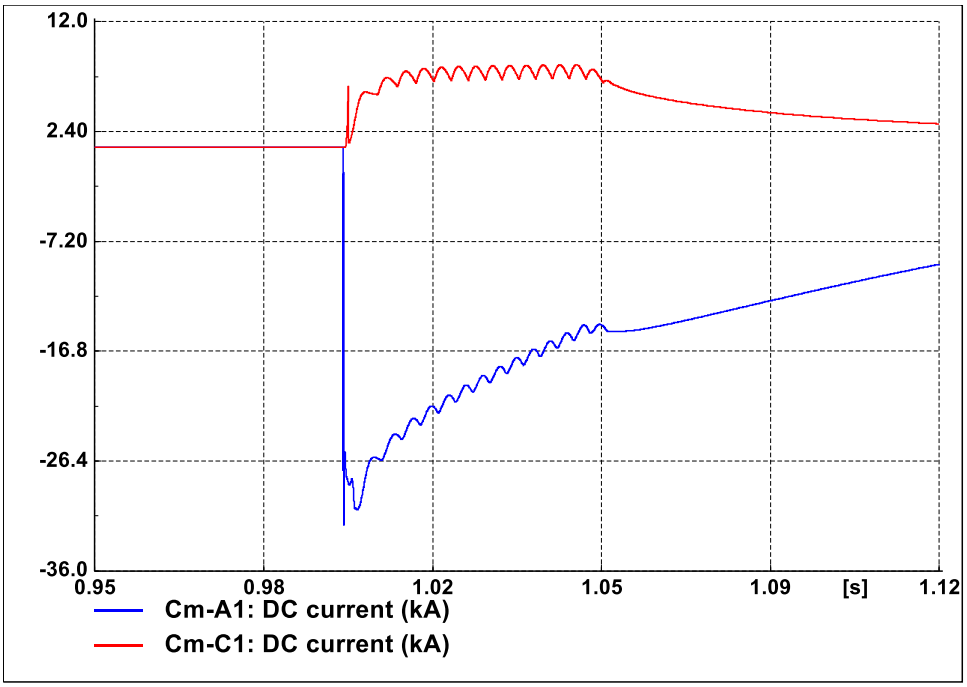

Figure 22: DC current at converter terminals Cm-A1 and Cm-C1.

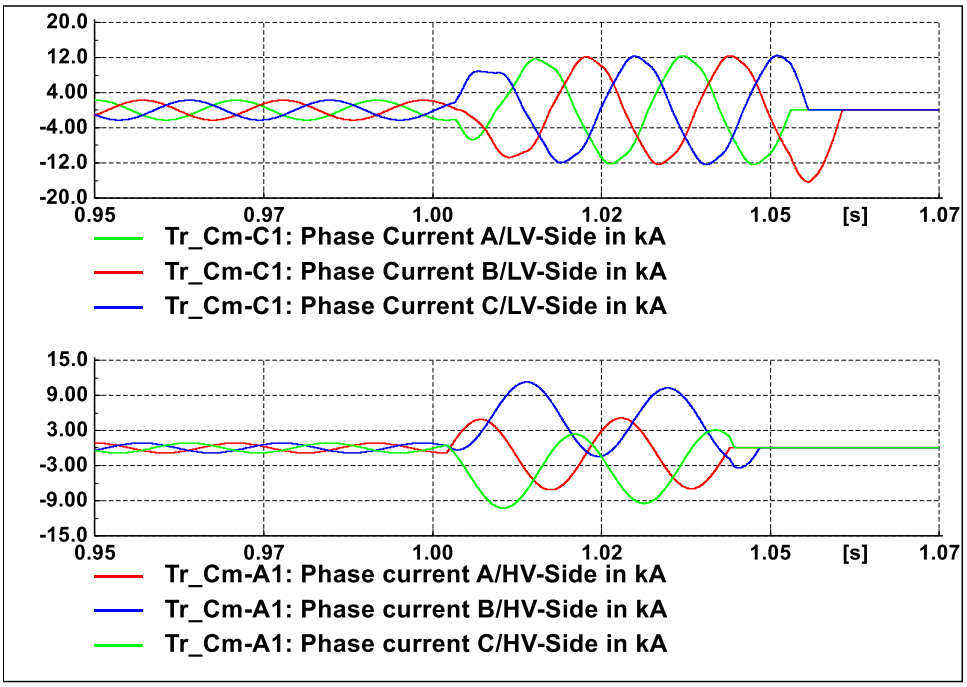

Figure 23: 3-phase instantaneous currents on primary side of transformer Cm-C1 (top) and Cm-A1 (bottom)